**Ex No: 04**

**Date: 18.10.2024**

**DESIGN OF CMOS D - FLIP FLOP AND MASTER SLAVE D - FLIP FLOP**

**AIM:**

To design and implement CMOS D-Flip Flop and Master Slave D – Flip Flop using Cadence Virtuoso 90nm CMOS technology

**TOOLS REQUIRED:**

Cadence Virtuoso Analog Design Environment

**PROCEDURE:**

* + - * Open Virtuoso and create a new library with existing gpdk090nm technology.
      * File -> New -> Cellview -> Schematic
      * With the help of the circuit diagram, implement the D-Flip Flop using cmos by adding instances and connect the instances using wire
      * Add the source and ground to the required pins
      * Complete the circuit with the wireconnections
      * Launch ->ADE L
      * Choose Transient analysis

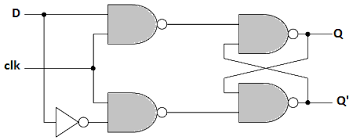
Set the stop time

Click on moderate

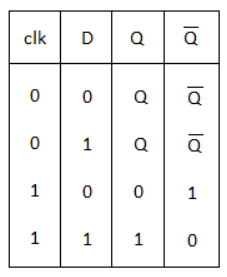
* + - * Select input and output pins from the design by clicking on the corresponding wires
      * Then run the simulation process to get the transient response
      * Thus, the pre layout simulation results are obtained

**CIRCUIT DIAGRAM AND TRUTH TABLE:**

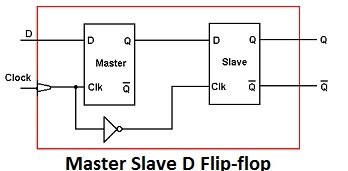
1. **D – Flip Flop:**



**Fig 4.1 Circuit diagram of CMOS D-Flip Flop**

 **Table 4.1 Truth Table for D-Flip Flop**

1. **Master Slave D – Flip Flop:**



**Fig 4.2 Circuit diagram of Master Slave D – Flip Flop**

A group of dots on a white background

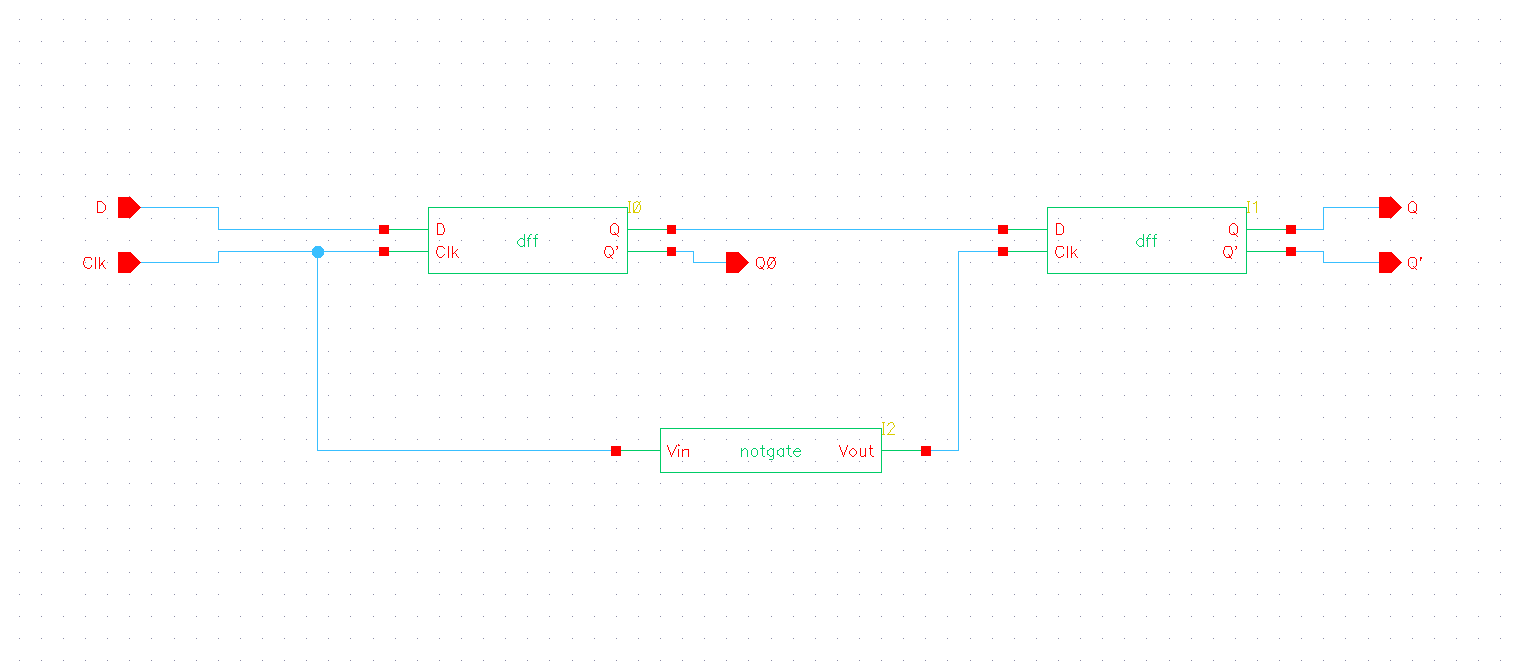
Description automatically generated**TRANSIENT ANALYSIS:**

**Fig 4.3 Schematic diagram of CMOS D-Flip Flop**

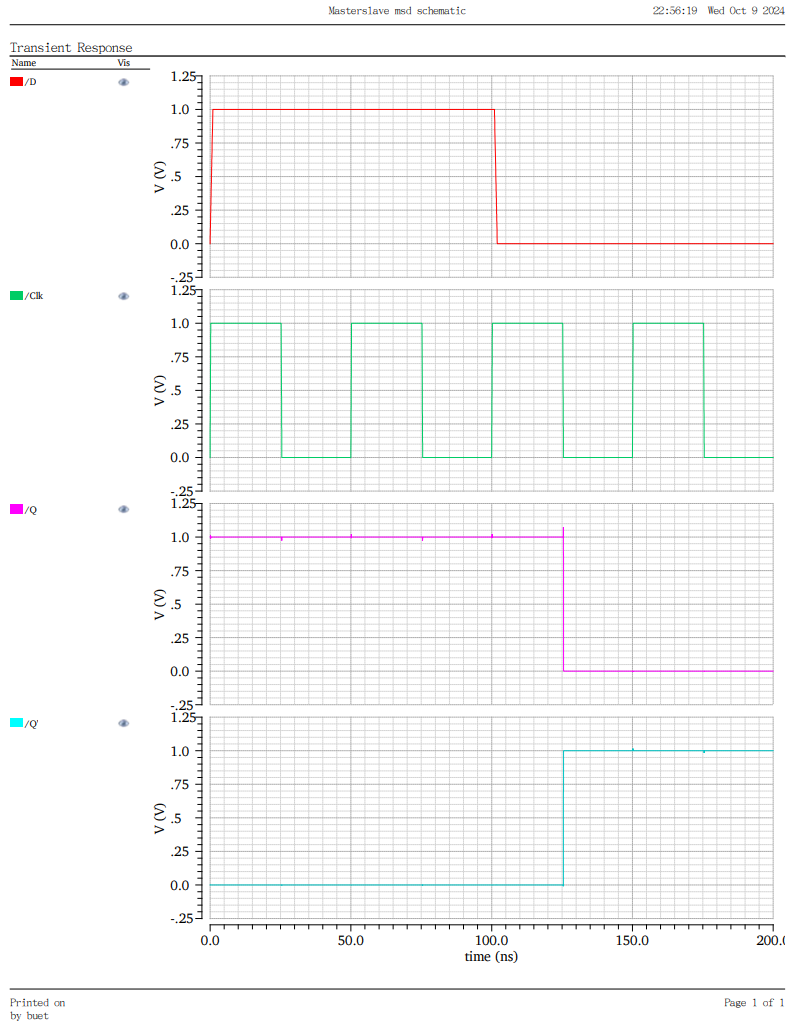
A screen shot of a graph

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**Fig 4.3 Transient Analysis of CMOS D-Flip Flop**



**Fig 4.4 Schematic diagram of Master Slave D – Flip Flop**

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**Fig 4.5 Transient Analysis of Master Slave D – Flip Flop**

**RESULT:**

Thus, the CMOS based D-Flip Flop was implemented and verified using Cadence Virtuoso Analog Design Environment.